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For

HOST FAIL-OVER SWITCH PRESENCE DETECTION COMPATIBLE WITH EXISTING PROTOCOL AND HOST CONTROLLERS

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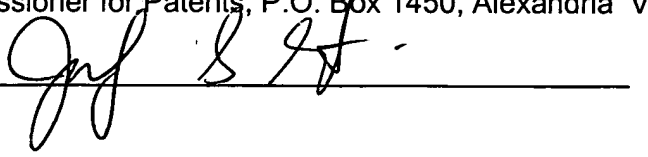

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Host Fail-Over Switch Presence Detection Compatible With Existing Protocol and Host Controllers

Field of Invention

[0001] The field of invention relates generally to detecting the presence of a host fail-over switch.

Background

[0002] A Serial ATA (AT Attachment) fail over switch (sometimes referred to as a "Port Selector") is a component that may provide two paths to a device (e.g., storage device), of which one is the selected/active port/connection. Upon detection by a standby system that the host or host controller communicating through the active port has failed, the active port is switched such that the standby system can take over and continue to have access to the storage device. This is a common approach taken in high-availability and redundant systems such as airline reservation systems, banking systems, and other mission-critical systems where continual up-time is a requirement.

[0003] The Serial ATA fail over switch as originally defined was completely transparent to both the device being accessed and the attached hosts. It was so transparent that its presence could not be directly detected and instead had to be inferred by attempting to cause it to switch and determining if a switch occurred. Furthermore, the fail over switch market requirements were that fail over switches be supportable with existing Serial ATA host controllers, so any new feature added to them must be benign/compatible with the controllers already on the market.

Brief Description of the Drawings

[0004] **Figure 1** presents a flow diagram describing the process of detecting a presence of a fail over switch, in accordance with one embodiment.

[0005] **Figure 2** illustrate a signal diagram showing the exchange of signals to identify the presence of a fail over switch, in accordance with one embodiment.

[0006] **Figure 3** presents a system diagram of a host and a device to exchange signals to identify the presence of a fail over switch, in accordance with one embodiment.

Detailed Description

[0007] In the following description, numerous specific details are set forth. However, it is understood that embodiments may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0008] Reference throughout this specification to "one embodiment" or "an embodiment" indicate that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0009] A method and apparatus for detecting a presence of a fail over switch is described. One embodiment provides a protocol transparent presence detection technique that allows the presence of a fail over switch to be determined by host controllers that support the detection technique, while remaining transparent to host controllers that do not have support for the detection signal. One embodiment allows detection to be done without adding any additional signals or wires to the fail over switch.

[0010] One embodiment of the presence detection signal uses a signal of the general Serial ATA initialization handshake sequence as defined in the

Serial ATA 1.0 specification. In that sequence, a number of handshakes are defined to complete the entire sequence. To make the sequence robust in the face of various transients and to accommodate such things as impedance calibration, the protocol of the Serial ATA specification is insensitive to reception of any signals other than the specific handshake signals expected.

[0011] In one embodiment, during the device presence handshake phase of the initialization sequence (where the host is defined in the Serial ATA specification to be insensitive to received signals other than the specific next handshake signal), an OOB (out of band) signal, other than the one the protocol calls for, is inserted, in accordance with one embodiment. This additional signal is ignored by current hosts but can be detected by host controllers that support fail over switch presence detection, in accordance with the description herein. After the newly inserted OOB signal, the traditional OOB handshake signals are transmitted to complete the handshake. A host capable of presence detection would detect the reception of the additional OOB signal and use that as indication of the presence of a fail over switch, while existing hosts that do not comprehend this signal would ignore it.

[0012] **Figure 1** presents a flow diagram describing the process of detecting a presence of a fail-over switch, in accordance with one embodiment. The processes of **Figure 1** are described in reference to the signal diagram of **Figure 2** and the system of **Figure 3**. The description below describes the transmission of signals compatible with the Serial ATA 1.0 specification. In alternative embodiments, if a host and device are communicating in accordance

with a separate protocol or specification, alternative signals could be used in place of the signals described below.

[0013] In process 102, the host 302 initiates a handshake initialization sequence with the device 304. In one embodiment, the host 302 transmits a COMRESET signal 202. In accordance with the Serial ATA 1.0 specification, the next signal transmission in the handshake sequence would be the device 304 responding with a COMINIT signal 204. However, in process 104, in one embodiment, the switch 306 inserts an OOB signal 206 to notify the host 302 of the presence of the fail over switch 306. In one embodiment, the inserted OOB signal 206 is a COMWAKE signal. In one embodiment, a unit of logic 307 within the switch 306 would identify the initial COMREST signal 202 being transmitted to the device 304 to initiate the handshake sequence, and the logic 307 of the switch would have the signal 206 transmitted to the host before conveying the device response to the initial signal to the host.

[0014] In alternative embodiments, alternative signals could be used in place of the COMWAKE signal. In yet another alternative embodiment, the switch may not transmit the inserted signal 206. Rather, the device 304 may send an OOB signal 206 to the host prior to sending the COMININT signal 204, to identify the presense of the fail over switch 306. Furthermore, in yet another alternative embodiment, the inserted signal 206 may be an in band signal.

[0015] In process 106, the host 302 receives the OOB signal 206 from the device. In process 108, a determination is made on whether the host 302 is of a

first set of hosts, or is of a second set of hosts. In process 110, if the host 302 is of a first set of hosts configured to read and identify the inserted signal 206 as identifying the presence of a fail over switch 306, the host 302 then identifies the presence of a fail over switch 306 accordingly. In process 111, if the host 302 is of a second set of hosts not configured to read and identify the inserted signal 206 as identifying the presence of a fail over switch 306, the host 302 then ignores the signal 206.

[0016] Thereafter, the handshake sequence continues in accordance with the pre-established protocol. For example, the case of the Serial ATA 1.0 specification, in one embodiment, in process 112, the device 304 transmits a COMINIT signal 204 to the host 302. In process 114, the host 302 responds with a COMWAKE signal 208 to the device 304. In process 116, the device responds to the host with a COMWAKE signal 210.

[0017] The processes discussed above can be stored on a machine-accessible medium. Thus, a machine- accessible medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form accessible by a machine (e.g., a computer, network device, personal digital assistant, manufacturing tool, any device with a set of one or more processors, etc.). For example, a machine-accessible medium includes recordable/non-recordable media (e.g., read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; etc.), as well as electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc -

[0018] In one embodiment, logic 307 of switch 306 and logic 310 of the host, are provided to support and perform the sequence as described herein, could be embedded as internal logic of a circuit or implemented with an integral state machine a circuit , in the host 302, switch 306, and/or the device 304. Having the sequence embedded in the logic of a circuit, and/or implemented in an integral state machine of a circuit, may also be referenced as being stored on a machine-accessible medium.

[0019] In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.